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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. 10/007,300
Filing Date ..... November 8, 2001
Inventor ..... Keiji Jono et al.
Assignee ..... Micron Technology, Inc.
Group Art Unit 2811
Examiner ..... T.F. Tran
Attorney's Docket No. KM1-003
Title: Methods of Forming an Isolation Trench in a Semiconductor, Methods of Forming an Isolation Trench in a Surface of a Silicon Wafer, Methods of Forming an Isolation Trench-Isolated Transistor, Trench-Isolated Transistor, Trench Isolation Structures Formed in a Semiconductor, Memory Cells and DRAMS

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Reference –See Attached Form PTO-1449

The Examiner's attention is directed to the reference which is listed on the attached Form PTO-1449, a copy of which is attached. No admission is made regarding whether the submitted reference is prior art.

Citation of the referenced art is respectfully requested.

Respectfully submitted,

Dated: 6-13-03

By: _____
D. Brent Kenady
Reg. No. 40,045